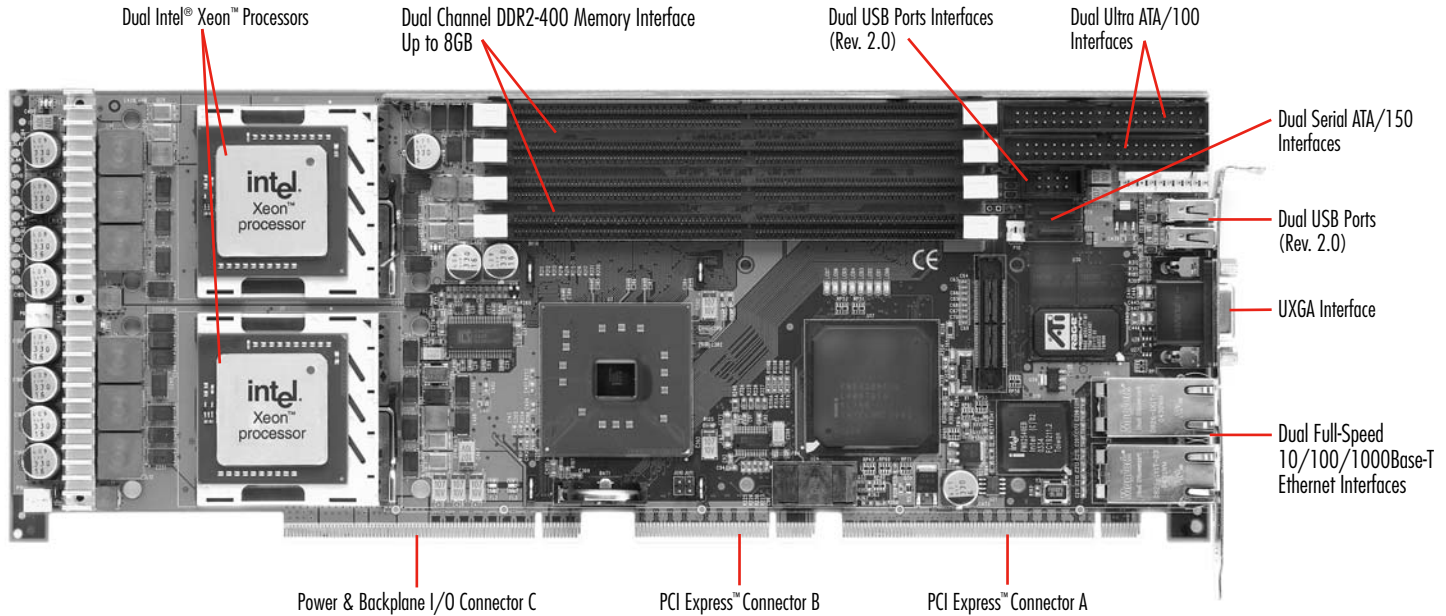


NLT (SHB Express™) SYSTEM HOST BOARD



Chassis Plans' NLT system host board turns the promise of PCI Express™ into a reality. The high-speed SHB-to-backplane PCI Express links employed on the NLT strip away parallel bus bandwidth limitations while unleashing the processing power of the next generation Intel® Xeon™ processors. The NLT features the Intel® E7520 chipset, an 800MHz system bus, dual DDR2-400 memory interfaces, dual Gigabit Ethernet ports and advanced video. PCI Express, PCI and PCI-X option card support makes the NLT an ideal choice for current as well as future industrial computing applications.

PROCESSORS:

Dual Intel® Xeon™ Processors at 2.8GHz to 3.6GHz*
 Processor Package: FC-mPGA4 (604-pin)

*Higher speeds as available

The Intel® Xeon processors used on the NLT support an 800MHz system bus as well as the Intel® NetBurst™ micro-architecture. These new processors support both 64-bit and 32-bit applications. Intel® Extended Memory 64 Technology (Intel® EM64T) is the processor feature that allows 64-bit application support. Other processor features:

- Hyper-Threading Technology
- Streaming SIMD Extensions 2 & 3 (SSE2 & SSE3)
- Hyper-Pipelined technology
- 1M Advanced Transfer Cache (L2) (2M L2 Cache - Future)
- 16K Level 1 data cache (L1)

CHIPSET:

Increased system performance is made possible by the Intel® E7520 chipset's ability to support an 800MHz system bus. The chipset configuration on Chassis Plans NLT board supports two registered DDR2-

400 memory channels. Data bottlenecks are reduced by the three PCI Express™ interfaces that provide high bandwidth (4GB/s) connections between the ports on the Memory Controller Hub (MCH) and external I/O devices or option cards.

PCI EXPRESS™ INTERFACES:

High-speed serial links that make up PCI Express interfaces typically have data rates twice that of PCI interfaces. A basic PCI Express link consists of at least one pair of differentially driven transmit and receive signal lines. PCI Express link bandwidth is increased linearly by adding signal pairs to form multiple lanes or wider lane widths. The most common PCI Express links used today are configured to have lane widths of x1, x4, x8 or x16. Chassis Plans' NLT system host board provides two x8 PCI Express links, one x4 PCI Express link and five PCI Express reference clocks on edge connectors A and B. These PCI Express links are used on SHB Express™ backplanes to support PCI Express option cards and bridge chips that provide PCI/PCI-X option card support. During system initialization the NLT automatically negotiates with the PCI Express cards connected to the PCI Express links in order to set up communication between the devices. The net result is that the NLT system host board supports communication to x1, x4, x8, x16 PCI Express boards as well as PCI/PCI-X cards via PCI Express-to-PCI/PCI-X bridge chip technology on the backplane.

DDR2-400 MEMORY:

The DDR2-400 interface is a dual channel interface originating at the Memory Controller hub with each channel terminating at two DIMM module sockets, for a total of four memory sockets. The NLT uses ECC registered PC2-3200 DIMMs and supports a maximum memory capacity of 8GB and a minimum memory interface bandwidth of 3.2GB/s per channel. The total effective memory interface bandwidth increases to 6.4GB/s when at least one PC2-3200 DIMM is used in each of the channels.

STANDARDS:

- PCI Express™ Base Specification 1.0a
- SHB Express™ System Host Board PCI Express Specification - PCI Industrial Computer Manufacturers Group (PICMG®) 1.3

PCI EXPRESS™ CONFIGURATION AND BUS SPEEDS:

- PCI Express - Edge Connectors A & B - Two x8 links, one x4 link
 - Five reference clocks
- PCI Express - (on-board only) - One x4 link
- PCI-X (on-board only) - 64-bit/66MHz
- PCI (on-board only) - 32-bit/33MHz
- Hub Link 1.5 - 266MB/s
- System or FSB - 800MHz

SERIAL ATA/150 PORTS (DUAL):

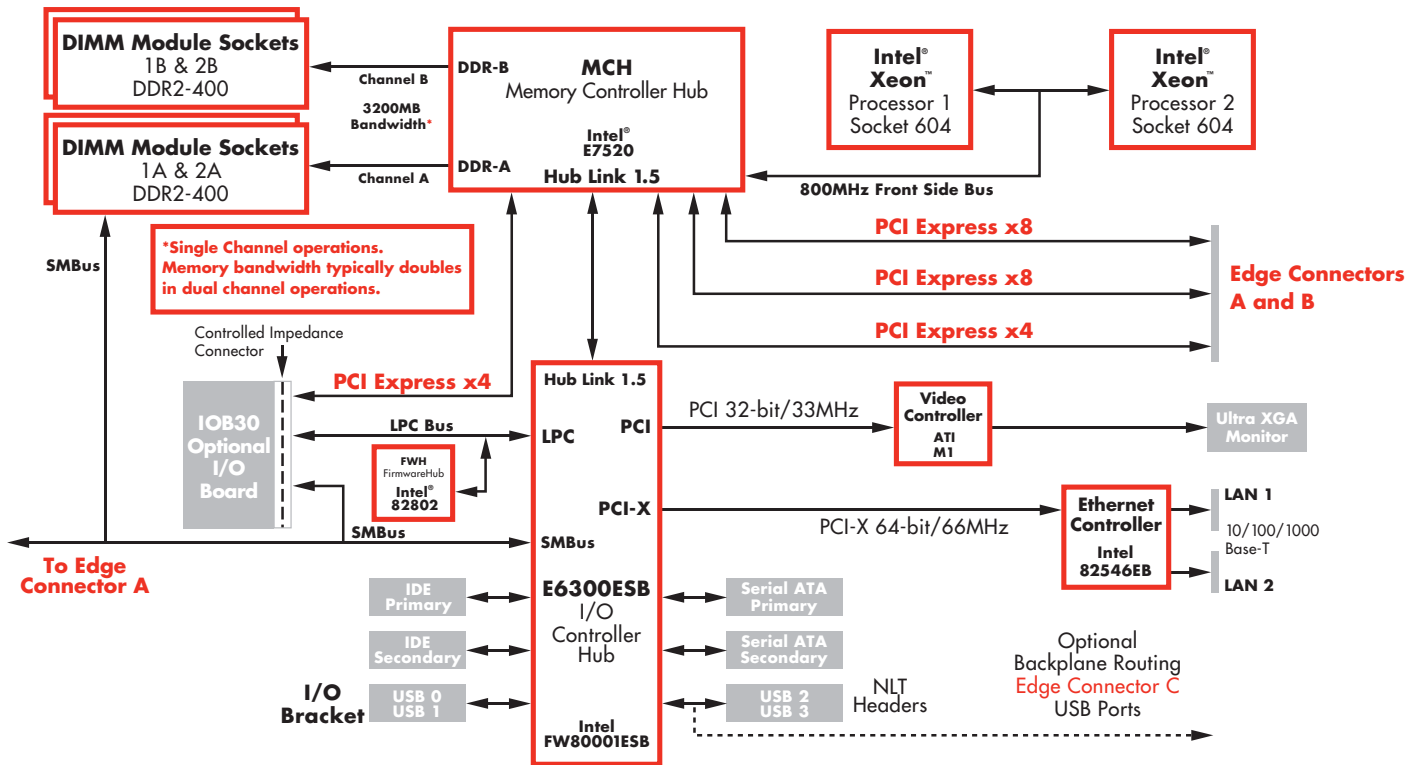
The primary and secondary Serial ATA (SATA) ports on the NLT boards comply with the SATA 1.0 specification and support two independent SATA storage devices such as hard disks and CD-RW devices. SATA technology provides lower-pin counts, reduced signaling voltages, simplified cabling, CRC error detection and hot-plug device support. SATA produces higher performance interfacing by providing data transfer rates up to 150MB per second on each port.

DUAL ETHERNET INTERFACES - 10/100/1000BASE-T:

The NLT uses an internal PCI-X bus to connect the I/O Controller hub to the Ethernet controller chip. This design feature provides high-speed dual Gigabit Ethernet on LAN ports 1 and 2. The SHB also supports 10Mb/s or 100Mb/s Ethernet networks. RJ-45 connectors on the I/O bracket provide the mechanical interface to the Ethernet networks.



The Original Industrial Computer Source™



ULTRA XGA INTERFACE:

The NLT is equipped with the third generation ATI® RAGE™ MOBILITY™ M1 video controller. The M1 enables 2D/3D video acceleration and provides 8MB of integrated video memory. In 2D mode the video controller supports pixel resolutions up to 1600 x 1200, and in 3D mode the maximum resolution provided is 1280 x 1024. The maximum color depth supported at these extremes is 16.7 million colors. Software drivers are available for popular operating systems.

QUAD UNIVERSAL SERIAL BUS INTERFACES (USB 2.0):

Two USB 2.0 interface ports are located on the I/O bracket of the NLT. Two additional USB 2.0 headers are available on the SHB. Ask Chassis Plans about optional USB routing to the backplane via NLT edge connector C.

BIOS (FLASH):

The NLT uses AMIBIOS®; the flash BIOS resides in the SHB's Firmware Hub (FWH). AMIBIOS8 contains features such as:

- Support for flash devices for BIOS upgrading
- Integrated support for USB mass storage devices such as USB, CD-ROM, CD-RW, etc.
- Boot from network, USB mass storage devices, IDE or ATAPI
- Serial port console redirection to support headless operation (requires optional IOB30, part number 6391-000)
- SATA/ATA/ATAPI support includes 48-bit LBA addressing to support SATA/ATA/IDE hard drive capacities over 137GB

AGENCY APPROVALS:

Designed for UL60950, CAN/CSA C22.2 No. 60950-00, EN55022:1998 Class B, EN61000-4-2:1995, EN61000-4-3:1997, EN61000-4-4:1995, EN61000-4-5:1995, EN61000-4-6:1996, EN61000-4-11:1994

NLT APPLICATION CONSIDERATIONS:

Power Requirements:

Typical Values			
CPU	+5V	+12V	+3.3V
3.6GHz	3.75A	17.00A	3.50A
3.2GHz	3.75A	15.40A	3.50A
2.8GHz*	3.75A	9.70A	3.50A

-12V @ <100mA

Tolerance for all voltages is +/- 5%

Temperature/Environment:

Operating Temperature: 0P to 45P C.

*LV Xeon operating temperature: 0P to 55P C.

Storage Temperature: -40P to 70P C.

Humidity: 5% to 90% non-condensing

Mechanical:

In a typical backplane, the NLT's cooling solution enables placement of option cards approximately 2.3" (58.4mm) away from the top component side of the SHB. The NLT's overall dimensions are 13.330" (33.858cm) L x 4.976" (12.639cm) H in accordance with the SHB Express full-length SHB dimension specification. The SHB Express™ board height specification is .176" (.447cm) taller than the PICMG 1.0 SBC height specification; however, relative PICMG 1.3 SHB height off the backplane is the same due to the shorter PCI Express backplane connectors.

ORDERING INFORMATION:

Model Name: NLT

Model #	CPU Speed
S6313-006-xM	3.6GHz
S6313-003-xM	3.2GHz
S6313-501-xM	2.8GHz

(xM = Memory)

ADDITIONAL NLT FEATURES:

System Hardware Monitor:

• The functions monitored are:

- Voltage: +3.3V, +/-12V, +5V and VCore
- Fan speed
- Temperature

I/O Features:

- Two EIDE Ultra ATA/100 interfaces
- Optional IOB30 I/O plug-in expansion board includes:
 - Enhanced bi-directional parallel interface
 - PS/2 mouse and keyboard interface (mini DIN connector)
 - Floppy drive interface
 - Two high-speed serial ports

Watchdog Timer:

- The programmable watchdog timer is supported directly by the I/O Controller Hub. Two operating modes, free-running and one-shot, are available with this two-stage watchdog timer. Stage one can generate IRQ, SMI or SCI. Stage two generates a programmable watchdog timer reset with a total range of 1ms to 10 minutes.

The stated bus speed, memory and communication interface speeds are component maximums; actual system performance may vary.

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